ABSTRACT

The speed of on-chip ADC testing of image sensors is increased by testing multiple chips in parallel. A wafer typically contains many individual image sensor chips. In a parallel on-chip test procedure, power is applied to a plurality of the image sensor chips and the chips are then tested in parallel. Additional power lines may need to be added to the wafer to allow power to be supplied to a plurality of the image sensor chips at once. These power lines may be etched directly on the wafer, or a wafer master may be used to overlay the wafer with the power lines for testing purposes. Additionally, test engines may be added to the wafer map to control the overall test procedures.

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